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Microporous silicon connected with silicon wires

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Abstract
Structures combining Si wires and porous Si (PS) were fabricated by a two-step method, in which chemical etching and electrochemical anodization were applied to obtain the silicon wires and PS, respectively. The Si wires can be retained due to the existence of the depletion layer during the electrochemical anodization. The structure of PS connected with silicon wires is attractive to realize effective electric contact on PS.

The observation of bright red photoluminescence (PL) from porous silicon (PS) has inspired numerous research groups worldwide to start investigations on PS in order to build Si-based light-emitting devices (LEDs) [1–3]. However, since the efforts of several years were insufficient to start fabrication of PS LEDs, certain pessimism became notable in considering PS as a suitable optoelectronic material [4]. Among the major problems of PS LEDs are their low quantum efficiency, slow performance and insufficient environmental stability. For instance, electroluminescence (EL) efficiency of so far existing PS-based devices is about two orders of magnitude lower than their PL efficiency [5], the root reason being the absence of reliable electrical contact to the rough surface of conventional PS [2].

Many efforts have been made to improve the electrical contact and current injection efficiency. For example, Barillaro *et al* fabricated a polysilicon n^+ film on top of an n^+-doped crystalline-silicon region as the current injector before the porous layer formation [6]; Nishimura and co-worker used alternately stacked nano- and meso-PS layers to decrease the series resistance [7]; and Gelloz *et al* proposed to from a low porosity superficial layer between porous silicon and the top contact [8, 9]. In this work, we present a new structure consisting of Si wires and PS layer, which can be realized by using a two-step technique, namely chemical etching followed by electrochemical anodization of Si wafer. As Si wires atop PS can provide a good electrical contact, we thus expect that the problem of short circuit through the rough PS surface can be solved.

The samples were prepared from p-type, B-doped, (110) oriented Si wafers with electric resistance of 10–12 Ω cm and impurity concentration 10^{16} cm^{-3}. The wafers were first chemically etched in aqueous solution of HF and $AgNO_3$, the concentrations being 3.0 M for the former and 14.0 or 5.0 mM (depending on the diameter of wires expected) for the latter. The treatment temperature was 50 °C and the etching time was 60 min. Following the chemical etching step, the samples were then put into diluted nitric acid (HNO_3: H_2O = 1:9 by volume) for four days to remove silver coating. Then, after rinsing with deionized water, they underwent electrochemical anodization in the mixture of HF, C_2H_5OH and H_2O with the volume ratio of 1:1.5:2; the current density being 30 and 20 mA cm^{-2} for the first 0.5 h and second 0.5 h, respectively. The specimens were examined in and Hitachi S-3500N scanning electron microscopes. Photoluminescence (PL) spectra were collected by using Hitachi F-4500 fluorescence spectroscope with excitation wavelength of 365 nm.

In the first, chemical etching, step, Si wires (see figure 1) were prepared by etching silicon plate in a HF–$AgNO_3$ solution, as was first proposed by Peng *et al* [10]. It was suggested that silicon substrate was etched as anode and provided electrons for reduction of Ag^+ species that formed dendrites on its surface. After a subsequent treatment by diluted nitric acid, most of the silver deposit was dissolved.

In the second, electrochemical anodization, step, a PS layer could form under the wires. Figure 2(*a*) shows the cross-sectional image of such a structure. The wafer for this specimen was etched with more concentrated solution (3.0 M HF and 5.0 mM $AgNO_3$) during the first step.

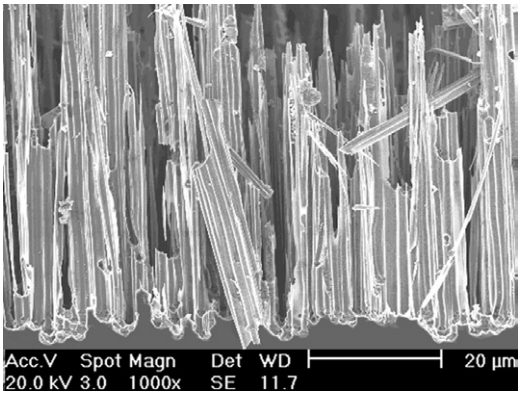

Figure 1. Silicon wires obtained by one-step chemical etching.

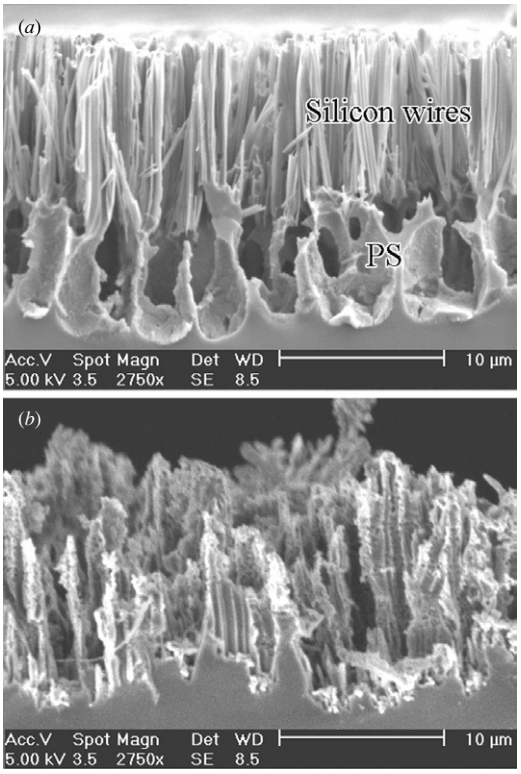

Figure 2. Different structures after electrochemical anodization (*a*) porous silicon covered with silicon wires by using thinner silicon wires; (*b*) PS-covered wires by using thicker (over 1 μm in diameter) Si wires.

Holes are necessary for the electrochemical reactions [3, 11]. In our experiments, holes are injected from the back side of silicon wafer by electrocircuit and then reach the bottom of Si wires. There, if the wires, which are soaked in electrolyte, are thick enough, holes can move along them and finally reach their tips, where the electrochemical anodization of Si occurs. However, if the wires' diameter is below two 'depletion layers', holes mainly move transversely and reach the interface between the wires and electrolyte, where they react with Si atoms and electrons, and thus are consumed at a very short distance. Such a phenomenon is called 'depletion' [12]. In this case, most part of silicon wires do not undergo electrochemical anodization and PS forms under the silicon wires, as well observed in figure 2.

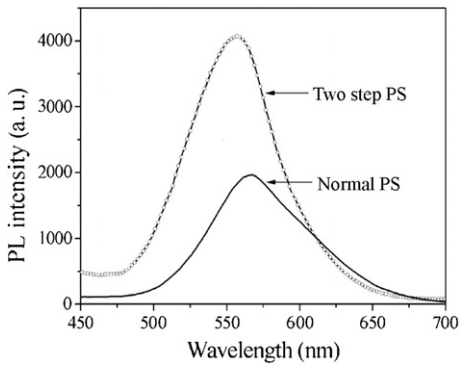

Figure 3. Photoluminescence spectra of normal PS and two-step PS.

The thickness of the depletion layer can be expressed by equation (1) [13],

$$d_s = \left[\frac{2\varepsilon_0\varepsilon_r V_D}{qN_A}\right]^{1/2} \tag{1}$$

where ε_0 is the dielectric constant of vacuum, $\varepsilon_r = 11.7$ is the dielectric constant of crystal silicon, V_D is the built-in potential whose value is determined as 0.64 V by comparing the work function of p-type Si and that of Ag remaining at the surface of silicon wires, $q = 1.6 \times 10^{-19}$ C is the hole charge and N_A is the ionized acceptor concentration, 10^{16} cm^{-3} for the Si wafers used. Taken together, the above data give a depletion-layer thickness of about 288 nm.

The threshold value of the diameter of Si wires was thus determined to be 576 nm, which is the thickness of two depletion layers. The silicon wires in figure 2 have diameter of 400–500 nm, i.e. less than the threshold value, therefore they kept unchanged during the electrochemical etching. The smoothness of the wires in figure 2 supports the above assumption.

In order to obtain Si wires thicker than the threshold value, a lower-concentration (3.0 M HF and 5.0 mM $AgNO_3$) etching solution was used in the chemical etching step. As a result, Si wires of over 1000 nm in diameter were produced. As expected and indeed seen in figure 2(*b*), during the electrochemical etching of such thicker wires electrochemical anodization occurred over their entire surface, leading to the formation of PS-coated Si wires. The result proves that holes did flow into thicker Si wires and caused electrochemical reaction at their surface.

We have performed PL measurement on the structure shown in figure 2(*a*). PL peak is hardly observed because Si wires at the surface do not emit light themselves and suppress such from PS by absorbing the stimulating light and PL from PS. However, once the wires are removed by ultrasonic vibration and PS exposed, the sample demonstrates strong PL intensity (figure 3), which is two times higher than that of normal PS produced by only electrochemical etching under the same preparation conditions. Such an improvement was reported to be the result of the high density of PS, its smaller nanocrystals in PS, and the existence of Si–Ag bonds on its surface [14]. The blue-shift of PL peak by ~10 nm can be attributed to the smaller Si nanocrystals on the surface of the two-step etched specimen [14]. The above results suggest a high-quality PS can be obtained by the two-step etching

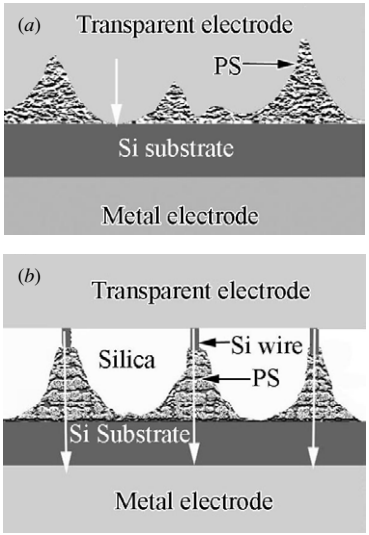

Figure 4. Schematic drawing of electric contacts in devices fabricated on top of (*a*) normal PS and (*b*) PS connected with silicon wires.

routine, although the Si wires may obstruct light emission from PS.

The structure of PS connected with Si wires (as shown in figure 2(*a*)) provides a possibility of making easy electrical contact and thus improving the efficiency of PS-based LEDs. As seen figure 4(*a*), conventional PS normally has rough surface. When a transparent electrode is directly deposited on the rough and uneven surface of such a PS layer [15], the current leakage may occur at the position where the PS layer is very thin, as marked by the white arrow. However, in the case of PS with Si wires, the PS poles almost have identical height, and are connected with Si wires, which are advantageous in making better electrical contact. As illustrated in figure 4(*b*), first, silica insulating layer can be deposited using CVD, PVD, or sol–gel methods on the PS to prevent the current leakage and improve the mechanical stability. Then the surface can be grinded to dismantle excessive length of the wires so that photons can emit easily from PS and obtain a plane with exposed wire tips. The grinding process can be monitored by PL analysis, where PL intensity should increase with the shortening of silicon wires, and the grinding stops once PL intensity becomes stable. Finally, a transparent ITO electrode can be deposited onto the surface. Due to the self-alignment of silicon wires with PS poles, electric current can be injected into the PS poles through the Si wires, and thus short circuit can be avoided. Consequently, one can anticipate that the structure in figure 4(*b*) will facilitate the effective injection of electrons and holes into PS and thus improve its EL efficiency. In the above design, we combine a good electric contact to PS and its superior quality achieved owing to the two-step production technique. As the obstruction effect of the Si wires is overcome by dismantling their most part, one can expect outstanding properties from the new-type PS LEDs.

In summary, structures combining Si wires and high-quality PS were prepared by a two-step method, in which chemical etching and electrochemical anodization were applied to obtain the silicon wires and porous silicon, respectively. It is shown that, depending on experimental conditions and then the size of Si wires, various combinations of PS and Si wires can be obtained, including PS connected with Si wires and Si wires covered with PS. A new device design based on the structure of PS connected with Si wires is proposed. The design is expected to realize reliable electric contact and be an effective way to improve the light-emitting efficiency of PS-based LEDs.

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