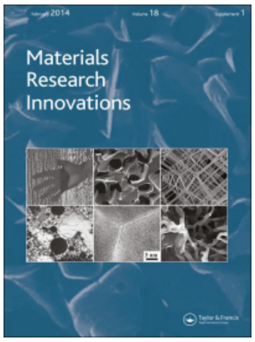

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Anisotropy of the conductivity of silicon nanowires

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ABSTRACT

This study reports the findings from an investigation into charge carrier transport within a silicon nanowire layer. The samples were prepared using the metal-assisted chemical etching method applied to crystalline silicon wafers with a resistance of 10–20 Ω·cm. The resulting silicon nanowires had a diameter of about 100 nm with a resistance of approximately 15 kΩ·cm. Electrical conductivity measurements were performed in both planar and sandwich configurations, revealing analogous conductivity mechanisms across different geometries. Frequency-dependent conductivity studies unveiled the presence of hopping conductivity. A hypothesis is proposed regarding the existence of a potential barrier at the interface between the nanowire layer and the substrate.

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Silicon nanowires; metal-assisted chemical etching; impedance spectroscopy; volt-ampere characteristic; structural and electrical characterisation

Introduction

One of the rapidly advancing domains in contemporary physics focuses on exploring the electrical and photoelectric properties of semiconductor low-dimensional systems. The study of silicon nanostructures is particularly significant, given silicon's pivotal role as the cornerstone of modern semiconductor electronics [1].

Silicon nanowires (SiNWs) have diverse applications, particularly in the detection of bacteria and viruses [2–4]. The interaction between organic molecules and the SiNW surface induces alterations in their electrical characteristics [5–7]. SiNWs also find utility in the development of micro-supercapacitors [8], battery electrodes [9] and solar cells [10,11]. The study by [12] underscores these potential applications and emphasises the prospect of modifying the electrophysical properties of SiNWs to enhance their efficacy in battery components.

The prevailing method for SiNW production is metal-assisted chemical etching (MACE). SiNWs generated through this method exhibit an exceptionally low thermal conductivity (~0.1 W/m·K), three orders of magnitude lower than that of the original crystalline silicon (c-Si) [13]. The feasibility of further doping pre-existing SiNWs opens avenues for employing these nanowires as thermoelectric converters [14]. Additionally, the samples referenced in [2–4,7] were obtained using this method. However, anisotropy of conductivity was not investigated in those studies.

All the applications mentioned above utilise the electrical properties of SiNWs. However, SiNWs exhibit strong anisotropic characteristics, with their overall electrical properties and conductivity being significantly dependent on the direction of charge carrier propagation within the structure. It is important to note that the conductivity along the nanowires may differ significantly from that across the nanowires. Although porous silicon has been extensively studied [15–17], there has been less research on structures made of nanowires. This study aims to investigate the conductivity characteristics of vertically aligned SiNWs under various contact configurations in both direct and alternating current.

Materials and methods

Sample preparation

SiNWs were synthesised using the MACE method on a p-type conductivity (100)-oriented crystalline silicon (c-Si) wafer with a resistivity of 10–20 Ω·cm Prior to the process, the c-Si wafer underwent thorough cleaning, involving rinsing in acetone and isopropanol in an ultrasonic bath. Subsequently, it was treated with 5 M HF to remove the oxide layer. The cleaned c-Si wafer was then immersed in a solution containing 0.01 M $AuCl_3$ and 5 M HF in a 1:1 volume ratio for 15 s, resulting in the deposition of gold nanoparticles on the c-Si surface. The gold-coated c-Si wafer was immersed in a solution of 5 M HF and 30% hydrogen peroxide in a 10:1 volume ratio for 30 min, causing etching in areas covered by gold nanoparticles. The removal of gold nanoparticles was achieved by immersing the sample in aqua regia (a solution of nitric (HNO_3) and hydrochloric (HCl) acids in a 3:1 volume ratio) for 5 min. SiNWs were formed at room temperature.

Structural characterisation of the obtained SiNWs was conducted using a Carl Zeiss SUPRA 40 scanning electron microscope (SEM).

Electrical characterization

The electrical characteristics of SiNWs were investigated through impedance measurements and volt-ampere characteristics. Aluminium contacts with dimensions of 1.5 × 3.4 mm were sputtered onto the samples at a distance of 1.2 mm using thermal sputtering on a VUP-5 setup. Two types of contacts were employed (Figure 1, contacts 1 and 2 - one type, contact 3 - the second type). For transverse conductivity investigation, contacts were sputtered on the nanowire surfaces (contacts 1 and 2), referred to as the planar configuration. For longitudinal conductivity investigation, contacts were also applied to the silicon substrate (contact 3), and a voltage was applied between the contact on the nanowire surface (contact 1) and the contact on the silicon substrate (contact 3), referred to as the sandwich configuration.

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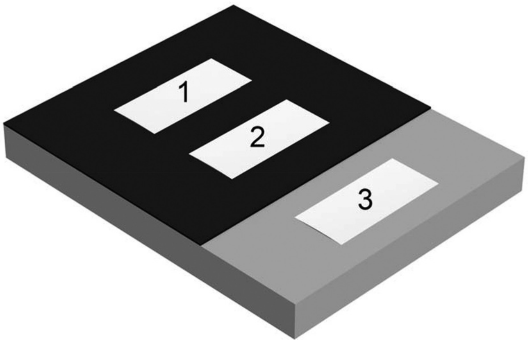

Figure 1. Sample image.

Measurement techniques

For alternating current measurements, an HP 4192A impedance analyser was utilised, operating in a frequency range from 10 Hz to 13 MHz. The applied alternating voltage had an amplitude of 0.05 V.

Direct current measurements were performed using a Keithley 6487 picoammeter-source. During volt-ampere characteristic measurements, voltage adjustments ranged from −10 V to 10 V in increments of 0.25 V, with measurements taken every 2 s.

All measurements were carried out at room temperature using the 2-probe method.

Experimental results

Microstructure analysis

Micrographs obtained through SEM (Figure 2) reveal quasi-ordered arrays of SiNWs predominantly aligned along the [100] crystallographic direction. The SiNW layer, post-etching, exhibits a thickness of approximately 13 µm (Figure 2b). Although individual nanowires have a diameter of ~100 nm, the considerable layer thickness causes nanowires to fuse, forming agglomerates of ~1–2 µm with inter-agglomerate distances of ~1 µm (Figure 2a).

Volt-ampere characteristics

Figure 3 illustrates the volt-ampere characteristic of the studied structures. The planar configuration displays a linear behaviour across the entire voltage range, exhibiting a conductivity of $0.28 \cdot 10^{-6}\ \Omega^{-1}$. According to our calculations, the specific resistance of the SiNW layer is approximately 15 kΩ·cm. Conversely, the sandwich configuration exhibits an asymmetric, rectifying behaviour resembling a diode-like volt-ampere characteristic. The diode behaviour is attributed to potential barriers [18] formed between the nanowires and the silicon substrate, possibly due to the adsorption of molecules on the nanowire surface and the capture of charge carriers by these molecules.

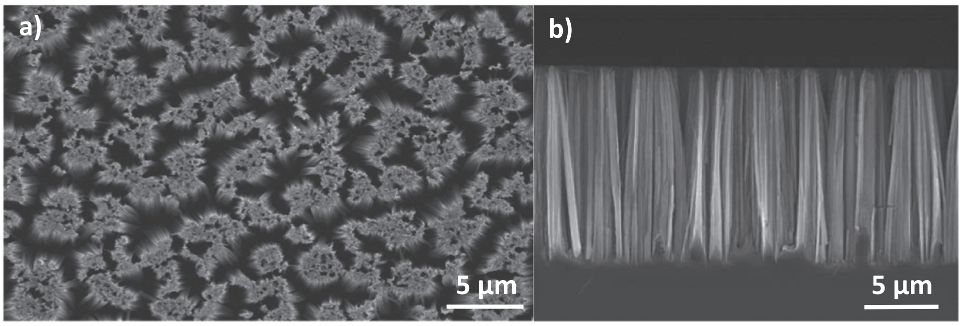

Figure 2. SEM images of SiNW sample a) top view, b) side view.

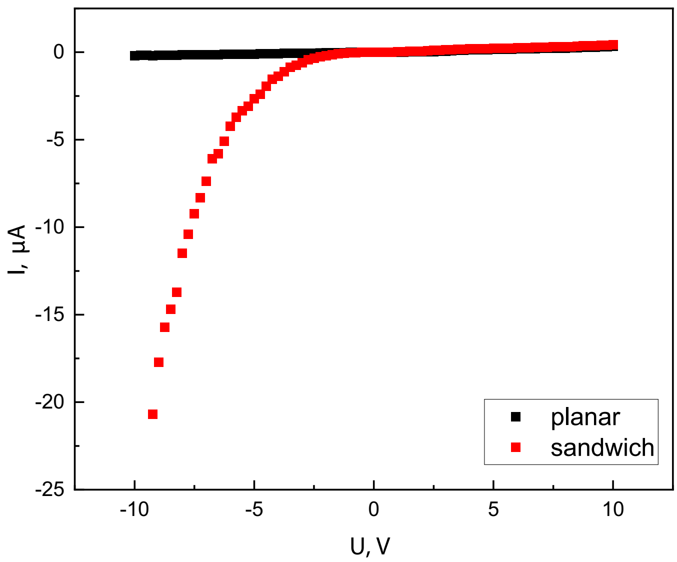

Figure 3. Volt-ampere characteristics of the sample.

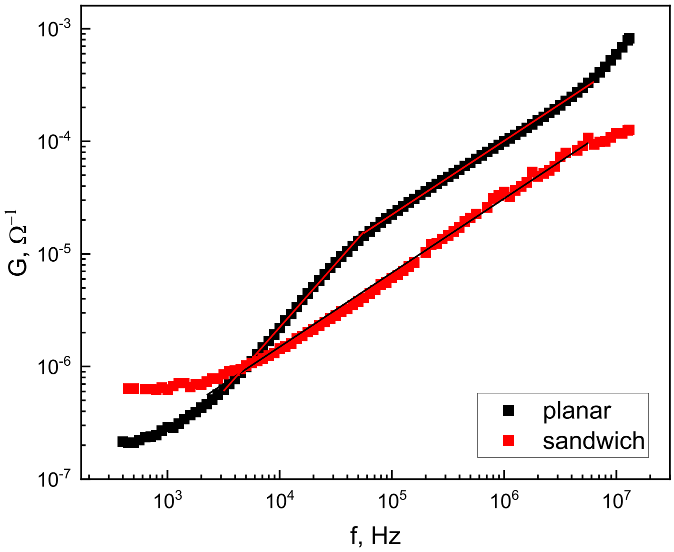

Figure 4. Frequency dependence of the conductivity of the samples. The red and black lines indicate approximations by the power law of conductivity (1).

Conductivity studies under alternating current conditions

To delineate variations in charge transport mechanisms between the planar and sandwich configurations, alternating current conductivity studies were conducted. Figure 4 illustrates the frequency dependence of conductivity in both configurations. In the sandwich configuration, the frequency dependence conforms to a power-law expression for hopping conductivity:

$$\sigma(\omega) = \sigma_0 + A\omega^s \tag{1}$$

where σ_0 – the baseline conductivity, A, s – constants, ω – the angular frequency of the alternating current.

An obtained parameter value of s = 0.66 is indicative of the hopping conductivity mechanism [19]. Conversely, the planar configuration exhibits a slightly different frequency dependence. On the frequency dependence of conductivity for a planar configuration, two power-law sections can be distinguished for low and high frequencies. At low frequencies, the parameter s takes the value 1.13, at high frequencies it is 0.66. The measurement error is less than 0.01. The fitting was implemented by the Levenberg-Marquardt algorithm.

The hopping conductivity mechanism implies that electrons in the nanowires traverse through localised energy levels induced, perhaps, by molecules adsorbed from the air [17,20].

Nyquist plots and impedance analysis

In Figure 5, Nyquist plots (hodographs) of impedance for the investigated samples are presented. The Nyquist plots are

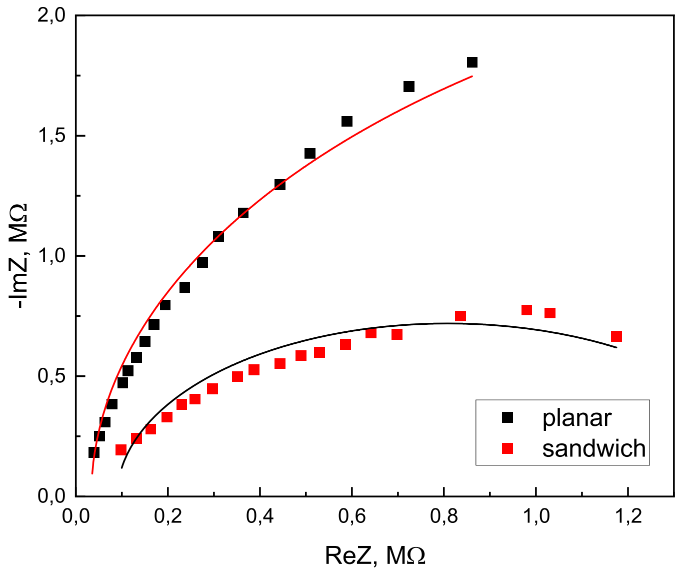

Figure 5. Nyquist plots of the impedance. The red lines and black indicate approximations.

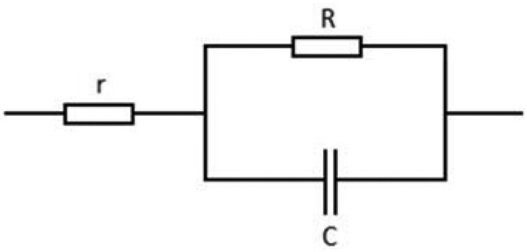

Figure 6. Equivalent circuit.

approximated by equivalent circuit shown in Figure 6. In this circuit, the resistor r represents the sample contacts. The resistor R accounts for the bulk resistance, while the capacitor C represents any capacitance present in the system. This equivalent circuit provides a simplified but still effective representation of the electrical characteristics observed in the experimental measurements.

By comparing impedance Nyquist plots across different sample configurations, specific patterns in the electrical properties of the nanowires are discerned. The similarity of Nyquist plots in the planar and sandwich configurations suggests the potential influence of common mechanisms or structural features on impedance.

Conclusions

SiNWs were synthesised using the MACE method on a c-Si substrate. The resulting SiNWs had a diameter of about 100 nm with a resistance of approximately 15 kΩ·cm. This study investigated the conductivity anisotropy of SiNWs and proposed differences in charge carrier transport mechanisms within these structures. In the planar contact configuration, the volt-ampere characteristic demonstrated a linear behaviour, while the sandwich configuration exhibited a rectifying form. A significant increase in conductivity is observed when a positive voltage is applied to the substrate base.

Both configurations displayed frequency-dependent conductivities approximated by a power-law, indicative of the hopping conductivity mechanism. However, a significant shift in the power occurred during the transition from the planar to the sandwich configuration. Equivalent circuits proposed for both configurations took the form of a simple parallel RC circuit connected in series with contacts resistance.

The observed alterations in the volt-ampere characteristic during the transition from planar to sandwich configuration are attributed to the formation of a potential barrier for charge carriers between the SiNWs and the c-Si substrate. This barrier is notably absent in the planar configuration, where the substrate does not participate in the charge carrier transport process.

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Disclosure statement

No potential conflict of interest was reported by the author(s).

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